CLAIMS

We claim:

1. A circuit comprising:

(a) a set of interconnected delay stages; and

(b) switch-controlled load circuitry connected to the output of one or more delay stages, wherein the switch-controlled load circuitry substantially shields the delay stages from noise in a power supply connected to the switch-controlled load circuitry.

2. The invention of claim 1, wherein the switch-controlled load circuitry is connected to the output of each delay stage.

3. The invention of claim 1, wherein the switch-controlled load circuitry selectively applies a load to the corresponding delay stage output.

4. The invention of claim 3, wherein the load comprises a capacitive load.

5. The invention of claim 1, wherein the circuit is an oscillator and the plurality of delay stages are connected in a ring.

6. The invention of claim 5, wherein the oscillator is a voltage-controlled oscillator, wherein the gain of each delay stage is a function of an applied control voltage.

7. The invention of claim 1, wherein, for each delay stage output, the switch-controlled load circuitry (1) is connected between the power supply and the delay stage output and (2) comprises a current source, a load, and a switch, wherein the switch is adapted to selectively apply the load to the delay stage output.

8. The invention of claim 7, wherein the impedance of the current source substantially decouples the load from the power supply.

9. The invention of claim 7, wherein the current source is a constant current source.

10. The invention of claim 7, wherein the load corresponds to a capacitance of a transistor.

11. The invention of claim 7, wherein:

the load corresponds to a gate-to-channel capacitance of a transistor;

the transistor is connected to the switch at a transistor gate node and to the current source at a first transistor channel node.

12. The invention of claim 11, wherein a second transistor channel node is connected to local ground.

13. The invention of claim 11, wherein the first transistor channel node is the transistor source.

14. The invention of claim 11, wherein:

the gate-to-channel capacitance corresponds to the gate-to-source capacitance of the transistor;

the current drain is connected to the transistor source; and

the transistor source is connected to local ground.

15. The invention of claim 11, wherein the transistor is an NMOS transistor.

16. The invention of claim 7, wherein:

each switch is adapted to be closed when an operating frequency of the circuit is below a specified threshold frequency; and

each switch is adapted to be open when the operating frequency of the circuit is above the specified threshold frequency.

17. The invention of claim 1, wherein:

the switch-controlled load circuitry is connected to the output of each delay stage;

the switch-controlled load circuitry selectively applies a capacitive load to the corresponding delay stage output;

the circuit is a voltage-controlled oscillator and the plurality of delay stages are connected in a ring, wherein the gain of each delay stage is a function of an applied control voltage;

for each delay stage output, the switch-controlled load circuitry (1) is connected between the power supply and the delay stage output and (2) comprises a current source, a load, and a switch, wherein the switch is adapted to selectively apply the load to the delay stage output;

the impedance of the current source substantially decouples the load from the power supply;

the load corresponds to a gate-to-channel capacitance of a transistor;

the transistor is connected to the switch at a transistor gate node and to the current source at a first transistor channel node;

each switch is adapted to be closed when an operating frequency of the circuit is below a specified threshold frequency; and

each switch is adapted to be open when the operating frequency of the circuit is above the specified threshold frequency.

18. A voltage-controlled oscillator comprising:

(a) a set of interconnected delay stages; and

(b) switch-controlled load circuitry connected to the output of one or more delay stages, wherein the switch-controlled load circuitry includes a transistor, a switch connected between a delay stage output and a gate node of the transistor, and a current source connected between a power supply for the transistor and a channel node of the transistor.

19. The voltage-controlled oscillator of claim 18, wherein the transistor is an NMOS transistor, the current source is connected to the drain node of the NMOS transistor, and the load corresponds to the gate-to-source capacitance of the NMOS transistor.

20. The voltage-controlled oscillator of claim 18, wherein the current source comprises a PMOS transistor.

21. A voltage-controlled oscillator comprising:

(a) a set of interconnected delay stages;

(b) a switch-controlled load connected to the output of one or more delay stages; and

(c) means for shielding the delay stages from noise in a power supply connected to the switch-controlled load.